

FORM PTO-1449 (SUBSTITUTE)		Attorney Docket No.: L&L-10178	Applic. No. 09/996,279
U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		Applicant Lothar Risch et al.	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (37 CFR 1.98(b))		Filing Date November 28, 2001	Group Art Unit

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U.S. PATENT DOCUMENTS

EXAMINER INITIALS		PATENT NO.	DATE	PATENTEE	CLASS	SUB CLASS	FILING DATE
<i>SK</i>	A	5,120,666	06/09/92	Gotou			
	B	5,646,058	07/08/97	Taur et al.			
	C						
	D						
	E						
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	I						

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		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUB CLASS	TRANSL. YES NO
<i>SK</i>	J	44 33 086 C2	03/30/95	Germany			X
	K	198 03 479 A1	12/24/98	Germany			X
	L	0 612 103 A2	08/24/94	Europe			X
<i>SK</i>	M	0 704 909 A2	04/03/96	Europe			X
	N						

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

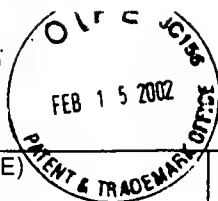
<i>SK</i>	O	Colinge, J.P. et al.: "Silicon-On-Insulator 'Gate-All-Around Device'", IEDM 1990, pp. 595-598
<i>SK</i>	P	Wong, Hon-Sum Philip et al.: "Self-Aligned (Top and Bottom) Double-Gate MOSFET with a 25 nm Thick Silicon Channel", IEDM 1997, pp. 427-430

EXAMINER	DATE CONSIDERED 7/29/02
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EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

	O	Pikus, F.G. et al.: "Nanoscale field-effect transistors: An ultimate size analysis", Appl. Phys. Lett. 1971, Vol. 25, December 22, 1997, pp. 3661-3663
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